ABSTRACT OF THE DISCLOSURE

A scanning circuit operates at a driving speed approximately twice the conventional speed when clock signals having the same frequency as those in the prior art are supplied. By alternately driving the switches in even-numbered and odd-numbered transfer stages T1 to Tn, the input side and the output side of each transfer stage are simultaneously made high in order of T1, T2, ... and Tn. Logical AND circuits are connected to the even- and odd-numbered stages to output pulse signals for scanning at intervals shorter than the clock period.